

Application of inkjet printing for 3D integration

Kim Eiroma, Heikki Viljanen; VTT Technical Research Centre of Finland; Espoo, Finland

Abstract

Inkjet printing is an attractive deposition tool to complement the traditional processing methods used in microelectronics integration. Its maskless, digital and non-contact nature provides many generic benefits, such as savings in processing steps and material usage, production flexibility and scalability to large areas. In addition, inkjet printing can be utilized in the integration of e.g. silicon and polymer or paper based systems, such as for the new wave of hybrid large-area, flexible devices, which are out of the scope of traditional clean room processing.

In this paper, we study the process of metallization of a Through-Silicon Via hole (TSV) by inkjet deposition. We describe the process of sample preparation and characterization. We finally demonstrate the creation of a fully inkjet printed 3D electrical interconnection using a Kelvin TSV test structure.

Introduction

Inkjet printing offers a unique approach to microelectronics 3D integration as it could provide a leap to maskless patterning and deposition to complement traditional microfabrication processes. Potential benefits are savings in processing steps and material usage, production flexibility, scalability to large areas, non-contact deposition on fragile layers or micro scale topographies and compatibility with a wide range of substrate materials for heterogeneous integration. The use of piezoelectric inkjet printing has previously been studied for over edge interconnections on chips and dies as a substitute for wire bonding [1], droplet based dispensing of micro bumps for flip chip bonding [2], and conductor dispensing for Through-Silicon Via (TSV) hole and redistribution layer metallization [3, 4, 5]. Industrial piezoelectric inkjet printing has similarly been applied for the fabrication of printed multilayer interconnections of epoxy-molded components in a system-in-package [6]. Other possible applications for inkjet printing in 3D integration include high accuracy adhesive material dispensing for attaching dies and building 3D topographies in the micrometer scale to assist in conductor patterning in subsequent processing steps. Inkjet also enables non-contact conformal patterning of insulation/passivation and encapsulation layers over 3D topography [7]. Ultimately, in combination with laser etched through-silicon via holes, inkjet printing could facilitate a fully maskless 3D integration process as it could replace three mask levels worth of cleanroom processing: deposition of conductor material into through-silicon via holes, patterning of the redistribution layer and deposition of flip chip bumps.

In this paper, we demonstrate the use of inkjet printing for deposition of a metal nanoparticle ink for creating a vertical electrical interconnection through a TSV hole. Forming an electrical contact over a sharp edge formed by wet etching on silicon is also studied as a reference to the TSV metallization process.

Experimental

Materials and equipment

Printing was performed using a PiXDRO LP50 advanced research printer from Roth & Rau driving an industrial piezoelectric multinozzle printhead with a nominal drop volume of 10 pL (SX3, Fujifilm Dimatix). The conductive ink used was a silver nanoparticle ink (DGP 40LT-15C, Advanced Nano Products) with solids loading of 30 wt-% dispersed in TGME (triethylene glycol monoethyl ether, b.p. 256 °C) as main solvent. Intermediate drying steps were performed offline using a hotplate (Linkam TMS 93) and final sintering of the printed samples was performed using a hot air oven.

The printing process optimization tests for TSV metallization were performed on Deep Reactive Ion Etched (DRIE) blind TSV structures with tapered sidewalls (sidewall angle 84°) and thermally grown silicon dioxide insulator. <100> silicon wafers were used in all the tests. The TSV fabrication process is described elsewhere [8].

Forming an electrical contact over a sharp edge was tested with wet etched silicon trenches (length 400 µm, height 110 µm and sidewall angle 54°).

Electrical testing of metallized Kelvin TSV test structures was done using tapered TSVs reaching through a 240µm thick substrate. In these test structures a low temperature deposited silicon dioxide was used as insulator material.

Through-silicon via hole and redistribution layer metallization process

Critical aspects in the TSV hole filling process were the via hole dimensions, droplet volume and printer accuracy, processing temperature and the strategy with which droplets were deposited into the hole. A large volume fraction of the nanoparticle ink is the carrier solvent which had to be removed during the filling process in order to obtain sufficient metallization thickness while preventing overfilling of the hole. Various filling strategies were applied for controlling this, mainly by varying the number of subsequent droplets and the deposition and drying delays and temperature. The effect of these strategies on the metallization quality after sintering was studied, using blind via holes with top diameter, bottom diameter, height, volume and pitch of 79 µm, 53 µm, 112 µm, 388 pL and 125 µm, respectively.

A single nozzle driven by jetting parameters optimized for stable satellite-free drop formation at 30 °C was used to deposit droplets into a row of 40 via holes within one printing swath. The printing resolution in the process direction was set to the pitch of the via holes and the cross process resolution was set to 1 µm (25400 dpi). The number of droplets deposited into a single via hole in one "set", i.e. the number of printing swaths in the process direction having a minimal cross-process directional inter-swath

shift of 1 μm , was then set by the width of the bitmap pattern in the print recipe. The deposition delay between subsequent droplets in a single via hole within a set was controlled by the printing speed in the process direction. The delay and substrate temperature during printing and between sets was controlled. Three different strategies (A, B, C) based on these process parameter combinations were tested (Table 1).

Table 1: TSV filling strategies and process parameters.

Strategies	A	B	C
Fill factor during set [%]	25	25	100
$T_{\text{substrate, deposition}}$ [$^{\circ}\text{C}$]	<i>moderate</i>	<i>high</i>	<i>low</i>
Drying between sets	<i>online moderate</i>	<i>online high</i>	<i>offline high</i>
Process parameters			
$T_{\text{substrate, deposition}}$ [$^{\circ}\text{C}$]	50	90	30
Inter-droplet delay [s]	5	1	1
No. of droplets in set	10	10	40
$T_{\text{substrate, inter-set}}$ [$^{\circ}\text{C}$]	50	90	150
Inter-set delay [s]	80	80	80
No. of sets	7	20	3
No. of droplets in total	70	200	120
t_{fill} for single TSV [min]	15	30	6

For strategy A, the via holes were partially filled during one set in order to minimize the required drying time at the moderate deposition substrate temperature used. In strategy B, the interdroplet delay was decreased from 5 to 1 second via increasing the deposition substrate temperature. The approach for strategy C was to completely fill the TSV hole at low deposition substrate temperature in order to maintain jetting stability. Prolonged printing over a heated substrate will typically modify or deteriorate the jetting performance of the ink which makes any high precision deposition challenging. An offline drying step at high temperature using the Linkam TMS 93 hotplate was then applied in between deposition sets. For both strategies A and B, the number of deposition sets until overfilling of the via holes was determined experimentally. For strategy C, the total number of droplets (120) was chosen from between that of strategies A and B (70 and 200, respectively). Oven sintering in air was performed for all printed samples at 175 $^{\circ}\text{C}$ for 90 minutes.

The process of forming an electrical contact over the sharp edge from the Redistribution Layer (RDL) onto the TSV hole side wall was first tested using the wet etched silicon trench samples. The process parameters for creating conductive single droplet wide lines printed over the trenches were optimized and intended as input for the RDL metallization. In these tests, the Linkam TMS 93 hotplate was fixed to the printer substrate table in order to be able to elevate the substrate temperature higher than that of the maximum of the printer substrate table.

The Kelvin TSV test samples were masked from the bottom side using a copper tape to enable filling of the TSV holes. Metallization of the via holes was then performed using strategy C. The number of droplets required in a set for complete filling of the

via hole volume was 175. The top redistribution layer was printed using the same ink as for the TSV metallization. Two layers were printed at a resolution of 650 dpi and substrate temperature of 30 $^{\circ}\text{C}$ with an offline hotplate drying step at 60 $^{\circ}\text{C}$ after each layer. After drying, the copper tape was removed and the bottom metallization, a line having dimensions of 0.2x2 mm connecting the TSV holes was printed using the same parameters as the top RDL layer. Finally, the sample was oven sintered in air at 175 $^{\circ}\text{C}$ for 90 minutes.

As a reference, a sample with bottom metallization using a flexo printable silver paste (Inktec TEC-PR-030) was prepared by manually doctor blading an approximately 50 μm layer of the paste connecting the bottom via hole openings. The paste was dried on a hotplate at 120 $^{\circ}\text{C}$ for 15 minutes.

Characterization

In order to optimize the inkjet process for the blind TSV structures, the deposited ink thickness and profile on the TSV sidewall was characterized. Both sample cross section polishing and Focused Ion Beam (FIB) cross section sample preparation techniques were avoided due to their relatively low through put and high price.

In order to be able to prepare the cross sections with a diamond pen, TSVs were arranged in a dense matrix like layout. On the TSV matrix structure, the TSVs were organized in vertical columns but in non-horizontal rows. When $\langle 100 \rangle$ silicon is cleaved with a diamond pen, the crack propagates along the $\{100\}$ crystal planes. Arranging the TSVs in non-horizontal rows made sure that the TSV rows are facing the $\{100\}$ crystal planes at an angle. This makes sure test structures cannot be cleaved without hitting TSVs. This is illustrated with a Scanning Electron Microscope (SEM) picture in Figure 1.

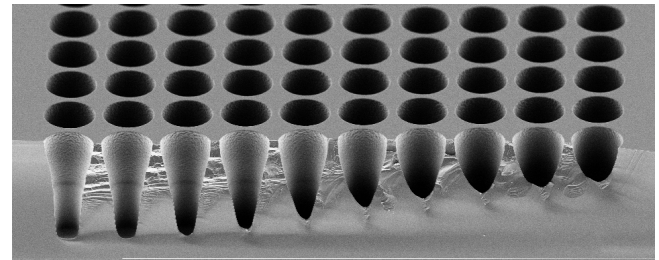


Figure 1. A TSV test sample cleaved with a diamond pen. The crack has propagated along the silicon $\{100\}$ crystal planes. Due to the mask layout the TSV rows are facing the $\{100\}$ crystal plane at an angle, which means that every TSV is cleaved from a different spot. The TSV pitch and top diameter are 50 μm and 45 μm , respectively.

The TSVs were first inspected with an optical microscope after inkjet printing and curing, then a SEM cross section was prepared and the cross section was imaged using a Carl Zeiss Supra 35 SEM.

In addition to the optical microscope and SEM, a Contour GT-X optical profilometer was used if the sample cross section preparation failed. In some cases the deposited ink thickness in the TSV was too thick to be cleaved along with silicon. Based on optical microscopy and SEM cross section alone, it was impossible to tell if the ink in the TSV was a solid truncated cone or a hollow

truncated cone. An example of optical microscope, SEM and optical profilometer pictures taken from the same sample is shown in Figure 2.

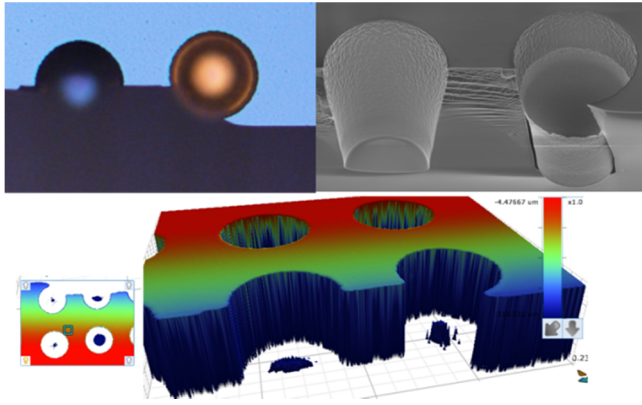


Figure 2. A failed cross section sample, where the sample was characterized with a combination of optical microscopy (upper left corner), SEM (upper right corner) and optical profilometer (below).

The described cross sectioning approach could not be used to cleave the Kelvin TSV test structures which consisted of only three TSVs. These cross section samples were first diced with a Disco DFD 651 dicing saw at the imminent vicinity of the TSV holes. The sample was then molded in epoxy and the diced surface was polished using a Struers RotoPol 22 polishing station.

The resistance of a single TSV was measured using a Kelvin TSV test structure. A 3D model for the structure is illustrated in Figure 3. In the Kelvin TSV structure, electrical current is fed from the left rear probe pad to the right rear probe pad. Current runs from the front side RDL through the TSV closest to the probe pads to the back side RDL and back up through the center most TSV. Two probe pads in the front are used to measure the voltage difference induced by the current going through the center most TSV.

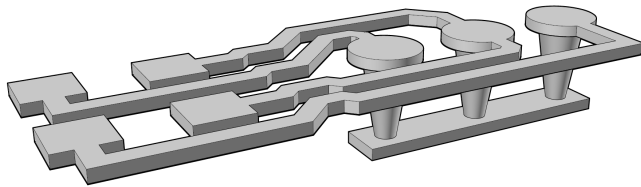


Figure 3. Kelvin TSV structure. The front side RDL has to be patterned, the only requirement for the back side RDL is that it is continuous.

Electrical characterization was performed using a Karl Süss probestation PA-150. Hewlett Packard 3476A multimeter was used in the four point probe measurements for the planar and trench test structures. For the Kelvin TSV characterization, Keithley 238 High current source measurement unit was used as current source and Hewlett Packard 3476A multimeter to measure voltage.

Results

Through-silicon via hole and redistribution layer metallization

Figure 4 shows SEM images of a cross section of the top left edge of the sidewalls of 79 μm top diameter blind TSV holes metallized using strategies A, B and C. The samples are representative of a larger number of samples processed using the same parameters.

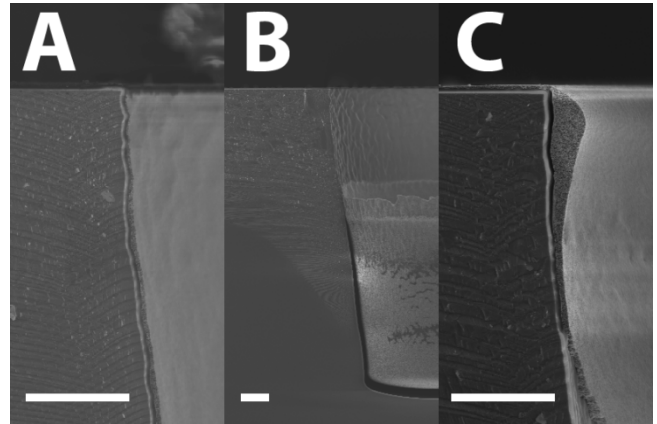


Figure 4. SEM images of a cross section of the top left edge of the sidewalls of 79 μm top diameter blind TSV holes metallized using strategies A, B and C. The scale bars are 10 μm .

Samples processed using strategy A showed good sidewall coverage with the material thickness decreasing towards the top edge of the via hole to less than 0.2 μm , the thickness at best being approximately 0.5 μm . Thinning of the metallization towards the top edge creates a challenge in achieving a continuous metallization over the edge to the top RDL. For strategy B, it is observed that even though the total number of droplets deposited is almost three-fold, the metallization fails to cover the side walls from approximately halfway towards the top surface. The effect is suggested to be due to the droplets instantaneously drying upon hitting the bottom of the TSV hole. The SEM image together with optical profilometer inspection suggests that most of the deposited material is at the bottom of the hole. In contrast, for strategy A, the polar silver ink seems to readily wet the hydrophilic silicon dioxide surface of the via hole prior to drying, with each deposited set of droplets with 25% fill factor building the metallization layer further towards the top surface. The metallization in strategy C shows an increase in the layer thickness towards the top edge from slightly less than 1 μm to 3 μm , effectively rounding off the sharp edge, for better continuity into the top RDL layer.

For comparison, an SEM image in Figure 5 shows a clean cross section of two blind TSV holes with top diameter, bottom diameter, height, volume and pitch of 58 μm , 31 μm , 99 μm , 159 pL and 75 μm , respectively, where the hole on the right has been metallized using the same strategy C. The hole on the left is left unfilled. Complete coverage of the sidewalls is obtained even though there is a slightly less pronounced increase in layer thickness towards the top edge and general variation in the layer thickness. The good coverage all the way to the top edge may be

attributed to the ink-sidewall contact line being at the very top of the sidewall at initiation of the inter-set heating phase. The temperature may be sufficiently large to induce a flow that drives the solute within the drying ink toward the contact line where the rate of evaporation of the solvent is highest, in analogy to the coffee ring effect [9]. However, this observation would have to be confirmed by further studies. In any case, it is evident that full coverage of the via hole sidewalls is obtained by strategy C, which is also the most rapid process for filling a single via hole as shown in Table 1.

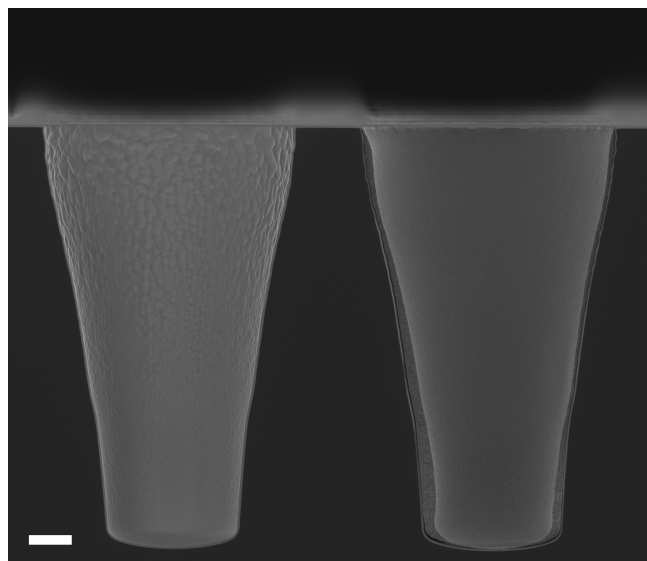


Figure 5. SEM image of a clean cross section of two blind TSV holes with top and bottom diameter, height, volume and pitch of 58 μm , 31 μm , 99 μm , 159 μL and 75 μm , respectively. The hole on the right has been metallized using strategy C, the hole on the left is unfilled. The scale bar is 10 μm .

The low deposition substrate temperature used in strategy C is beneficial for a stable jetting process which is a prerequisite for repeatable filling of small TSV diameters at small pitches. Repeatable selective filling of TSV holes down to 45 μm in diameter and 50 μm in pitch was demonstrated using strategy C. In Figure 6, showing an SEM image of a cross section of 10 blind TSV holes, the three outermost holes from the left and right were filled. The rough sidewall surface of the four unfilled TSV holes in the center can be clearly seen. The resolution limits are determined by droplet volume and drop placement accuracy, which is a product of droplet jetting stability and straightness and printer motion accuracy and repeatability.

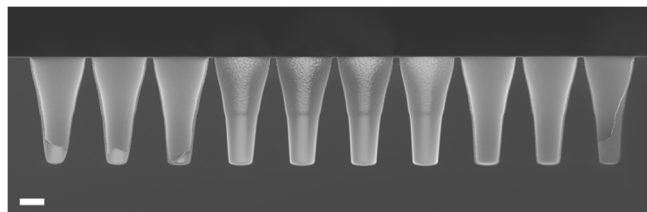


Figure 6. SEM image of a cross section of 10 blind TSV holes with top diameter and pitch of 45 μm and 50 μm , respectively. The three outermost TSV holes from the left and right are filled. The scale bar is 20 μm .

The TSV metallization for the Kelvin test structures was deposited using strategy C. Figure 7 shows a dSLR camera image of the test sample after TSV and top RDL metallization.

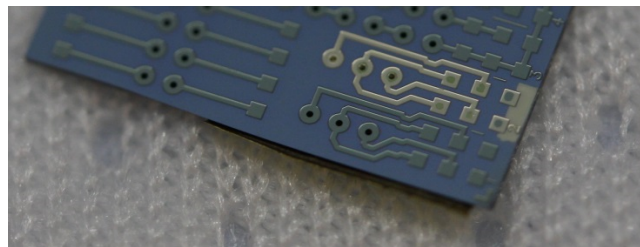


Figure 7. dSLR camera image of a Kelvin TSV test sample after TSV and top RDL metallization. TSV hole pitch is 600 μm .

An optical micrograph of a Kelvin TSV cross section sample with inkjet printed top RDL and TSV metallization, and bottom RDL coated using a flexo printable silver paste, is shown in Figure 8 (top). The image was stitched from multiple optical microscope images. A close up of the left most TSV is shown in Figure 8 (bottom). In both images the metallizations have been delaminated and rolled into the TSV during the sample preparation. The epoxy used in the moulding was too viscous to enter the hollow TSV structures and hence did not support the ink on the TSV sidewall during the cross section polishing. In any case, Figure 8 shows that despite the larger dimensions of the via holes, strategy C provided full coverage of the via hole sidewalls. This was confirmed also with electrical measurements.

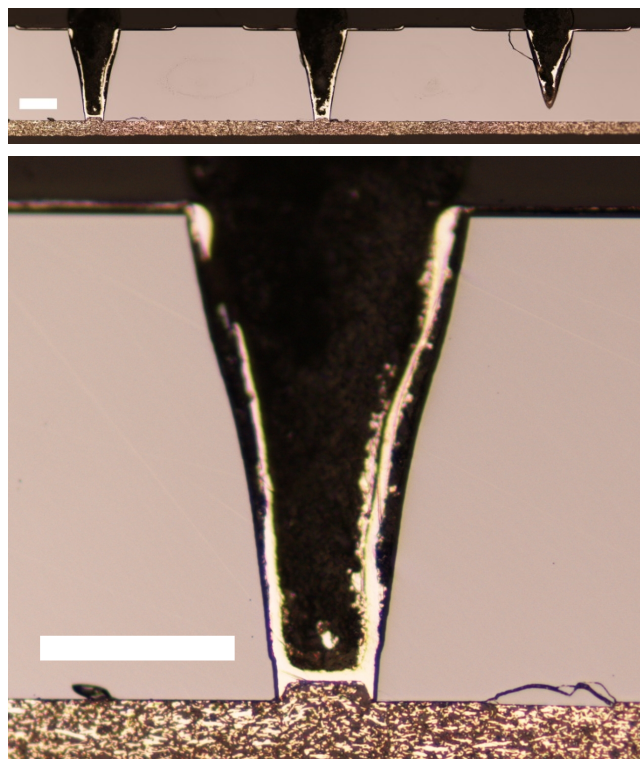


Figure 8. (top) A cross section image of the three TSV hole Kelvin test structure, and (bottom) a close up of the left most TSV. Scale bar is 100 μm .

Electrical characterization

As a reference, the ink jetted conductor was first measured from a planar surface where the ink was deposited by only one layer. A 1 cm long single pixel wide line had a resistance of 121 Ω . A conductor cross sectional area of 11 μm^2 was measured with the help of a profilometer. Based on the cross section and resistance, the resistivity of the silver ink was 13 $\mu\Omega\text{cm}$.

In the parameter optimization over the trench samples it was evident that the ink had a tendency to spread along the sharp edge due to capillary effects. Significant substrate heating was required in order to minimize the capillary spreading and to maintain sufficient conductor thickness at these critical points. At the same time, conductor thickness was maximized by increasing the print resolution. The optimized process (resolution 1200 dpi, substrate temperature 200 $^{\circ}\text{C}$ and printing speed 1 mm/s) leads to a coin stack type of morphology, as each subsequent droplet has time to dry prior to the next droplet being deposited.

When the electrical measurement was repeated with the trench structures, it was noticed that three layers were not enough to get a contact through the trench with the low angle sidewalls. When the amount of layers was increased to five, electrical contact was made.

Subsequent layers were printed by multidirectional swathes without a delay. Both 3 and 5 layer lines had a width of approximately 50 μm , although for the 5 layer line some spreading of the ink and roughening of the line edges was observed. Also, longer periods of the printhead scanning on top of the heated substrate will lead to jetting instability, which will deteriorate line quality.

With five layers the cross sectional area of the conductor was 145 μm^2 on the plane. The measured resistance for a 1 cm long conductor was 5.3 Ω . Based on the cross sectional area of the conductor on the plane, the resistivity in this structure is 776 $\mu\Omega\text{cm}$, over one order of magnitude higher than with the planar structure. This can be taken as an indication that the conductor thickness at the trench edge and on the sidewall is not the same as the thickness on the plane. Figure 9 shows an image of the trench test structure taken with a dSLR camera.

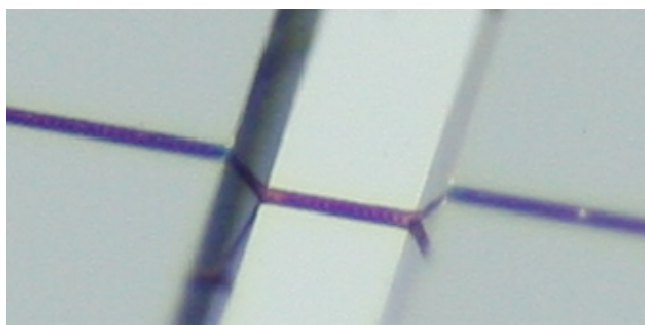


Figure 9. Picture of the trench test structure with inkjetted conductor line taken with a dSLR camera. The width and depth of the trench is 400 μm and 110 μm , respectively.

A SEM image of a 5 layer thick printed conductor at the edge of the trench sidewall and top surface is shown in Figure 10. Even with the optimized process parameters, some capillary spreading of the ink is observed. The stacked coin morphology of the conductor

is also evident, the solidified droplet appearing slightly oval due to the tendency of the ink to flow downwards along the trench sidewall.

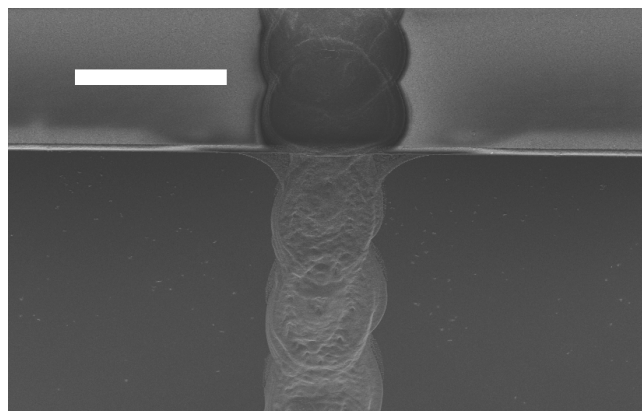


Figure 10. SEM image of 5 layer printed conductor at edge of trench sidewall (bottom) and top surface (top). The scale bar is 50 μm .

The poor conductivity over even the low angle trench structure hinted that either an extremely long deposition time (multiple layers passes) or a special process was needed for the steeper angle TSV structures. As explained earlier, process C was developed for this purpose. It was then used for the metallization of the Kelvin TSV via holes. With the optimized TSV filling process, eventually only two printed layers of the RDL at low temperature were needed to provide electrical contact. It is suggested that the thicker metallization layer at the top edge of the TSV rounded off the sharp edge and provided a support for a less demanding deposition process for the RDL layer than expected.

Kelvin TSV test structures with flexo printing paste RDL and ink jet RDL were characterized using two different currents. Measured voltages for 1 and 10 mA currents and the calculated resistances are recorded in Table 2.

Table 2: Measured voltages from the Kelvin via structures with two different currents and the calculated resistances.

	Current [mA]	Voltage [mV]	Resistance [$\text{m}\Omega$]
Silver ink	1	0.083	83
	10	0.831	83.1
Conductive paste RDL	1	0.774	774
	10	7.77	777

It was noticed that for the structure with the flexo printing paste, the resistance of the via was one order of magnitude higher. As identical deposition parameters were used for both test structures, the higher resistance is probably caused by the higher contact resistance.

Conclusions and Outlook

In our work we have investigated the use of inkjet deposition as a novel process for creating 3D electrical interconnections in microelectronic device integration. We have demonstrated the fabrication of a fully inkjet printed TSV electrical interconnection using a conductive silver nanoparticle ink. The resistance through a single Kelvin TSV via structure was calculated to be 83 mΩ.

The required low viscosity and solids loading of conductive inkjet inks present a challenge to achieving sufficient material coverage over sharp edges and non-planar surfaces. As shown, an optimized processing strategy can to some extent overcome these challenges. The long term reliability of inkjet deposited conductor metallization should be studied in more detail, but initial observations indicate that for example adhesion of the silver nanoparticle ink on the silicon dioxide surface is poor. Further studies should be devoted to the screening of multiple printable materials and to understanding the behavior and conversion of low-viscous inks to solid form on non-planar topography.

The deposition accuracy of current industrial piezoelectric inkjet systems, considering drop volume and the accuracy of the substrate transport, is in the order of tens of micrometers. In our experiments, reliable filling of TSV holes with a diameter and pitch of 45 μm and 50 μm, respectively, was at the limit of the process accuracy.

The ability to masklessly deposit multiple device layers using multiple materials at the same time is a promising feature of inkjet deposition. This agility and flexibility in production could make inkjet an attractive process at least as a tool in product development and for production of customized solutions.

Using industrial scale deposition systems having multi-printhead clusters and advanced process control, the process has the potential to be upscaled to a cost-effective production scale. A thorough analysis of the industrial scale applicability is however needed, taking the aforementioned issues of performance, reliability, throughput, yield and price into parallel consideration.

The integration of flexible polymer and silicon based devices is potentially an attractive application for inkjet printing. In order to realize interconnections from polymer to silicon, low temperature processes that are within the thermal budget of plastics such as polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), need to be developed. Here, selective laser sintering could for example be utilized. Laser sintering could also be used for the in-situ drying of filled via holes in order to avoid intermediate offline drying steps.

References

- [1] Mäntysalo, M., Li X., Jonsson, F., Yi, F., Lopez Cabezas, A., Li-Rong, Z., "System integration of smart packages using printed electronics," 62nd IEEE Electronic Components and Technology Conference (ECTC), pp. 997-1002. (2012).
- [2] Sadie, J., Subramanian, V., "Three-Dimensional Inkjet-Printed Interconnects using Functional Metallic Nanoparticle Inks," *Advanced Functional Materials*, 24(43), pp. 6834–6842. (2014).
- [3] Quack, N., Sadie, J., Subramanian, V., Wu, M.C., "Through Silicon Vias and thermocompression bonding using inkjet-printed gold nanoparticles for heterogeneous MEMS integration," *The 17th International Conference on Solid-State Sensors, Actuators and*

Microsystems (Transducers & Eurosensors XXVII), pp.834-837. (2013).

- [4] Rathjen, A., Bergmann, Y., Krüger, K., "Feasibility Study: Inkjet Filling of Through Silicon Vias (TSV)", *NIP28: International Conference on Digital Printing Technologies and Digital Fabrication*, pp. 456-460. (2012).
- [5] Khorramdel, B., Mäntysalo, M., "Inkjet filling of TSVs with silver nanoparticle ink," *Electronics System-Integration Technology Conference (ESTC)*, pp. 146-150. (2014).
- [6] Pekkanen, V., Mäntysalo, M., Kaija, K., Mansikkamäki, P., Kunnari, E., Laine, K., Niittynen, J., Koskinen, S., Halonen, E., Caglar, U., "Utilizing inkjet printing to fabricate electrical interconnections in a system-in-package," *Microelectronic Engineering*, 87(11), pp. 2382-2390. (2010).
- [7] Mengel, M., Nikitin, I., "Inkjet printed dielectrics for electronic packaging of chip embedding modules," *Microelectronic Engineering*, 87(11), pp. 593–596. (2010).
- [8] Dixit, P., Vähänen, S., Salonen, J., Monnoyer, P., "Effect of Process Gases on Fabricating Tapered Through-Silicon vias by Continuous SF₆/O₂/Ar Plasma Etching," *ECS Journal of Solid State Science and Technology*, 1 (3), pp. 107-116. (2012).
- [9] Derby, B., "Inkjet Printing of Functional and Structural Materials: Fluid Property Requirements, Feature Stability, and Resolution," *Annual Review of Materials Research*, 40(1), pp. 395–414. (2010).

Author Biography

Kim Eiroma (M.Sc. Tech) is a research scientist and expert in inkjet deposition for the fabrication of functional devices. He has worked at VTT since 2006 and has been involved in private and jointly funded projects covering a multitude of applications for printed functionality, such as printed antennas and metallization for e.g. optoelectronic devices, thin film transistor fabrication, microelectronic and hybrid integration, optical devices, diagnostics and product safety.